Glossary

February 1998

A

Altera Consultants Alliance Program (ACAP) An alliance created to provide expert design assistance to users of Altera programmable logic devices (PLDs). ACAP℠ consultants provide their expertise and services to designers.

Altera Hardware Description Language (AHDL) Altera's design entry language. A high-level, modular language that is integrated into the MAX+PLUS® II development system. You can create AHDL Text Design Files (**.tdf**) with the MAX+PLUS II Text Editor or any standard text editor, then compile, simulate, and program your projects within the MAX+PLUS II software. AHDL supports Boolean equations, state machines, and conditional and decode logic. AHDL also allows you to create and use parameterized functions, and includes full support for functions in the library of parameterized modules (LPM).

Altera Megafunction Partners Program (AMPP) An alliance between Altera and developers of synthesizable megafunctions. The AMPP℠ program was created to bring the advantages of megafunctions to users of Altera PLDs.

array clock A clock signal that passes through the logic array of a device before arriving at the clock input of a register.

Assembler The Compiler module that creates one or more Programmer Object Files (**.pof**), Jam Files (**.jam**), SRAM Object Files (**.sof**), Serial Vector Files (**.svf**), Tabular Text Files (**.ttf**), Hexadecimal (Intel format) Files (**.hex**), and optional JEDEC Files (**.jed**) for programming Altera devices.

Assignment & Configuration File (.acf) An ASCII file that stores information about probe, resource, and device assignments for a hierarchy tree, as well as configuration information for the Compiler, Simulator, Timing Analyzer, and Programmer. All information that can affect output files containing design information for the current hierarchy tree is controlled by the ACF.

B

BGA Ball-grid array. A device package offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* in this data book for more information.

BitBlaster Cable A serial download cable that allows both PC and UNIX workstation users to program and configure devices in-system or in-circuit. The BitBlaster™ serial download cable provides programming support for MAX® 9000, MAX 7000S, and MAX 7000A devices, and configuration support for FLEX® 10K, FLEX 8000, and FLEX 6000 devices. FLEX 6000 and FLEX 10K devices can be configured together in a FLEX chain; FLEX 8000 devices cannot be configured with other FLEX devices.

ByteBlaster Cable A parallel download cable that allows PC users to program and configure devices in-system. The ByteBlaster™ parallel port download cable provides programming support for MAX 9000, MAX 7000S, and MAX 7000A devices, and configuration support for FLEX 10K, FLEX 8000, and FLEX 6000 devices. FLEX 6000 and FLEX 10K devices can

be configured together in a FLEX chain; FLEX 8000 devices cannot be configured with other FLEX devices.

C

carry chain A dedicated architectural feature of the FLEX 10K, FLEX 8000, and FLEX 6000 device families that provides a high-performance carry-forward function between logic elements (LEs). The carry-in signal from a lower-order bit moves forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This carry-forward function is ideal for adders, counters, and comparators.

cascade chain A dedicated architectural feature of the FLEX 10K, FLEX 8000, and FLEX 6000 families that allows implementation of high-performance, wide fan-in functions. Adjacent LUTs can be used to compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain is available only in FLEX 10K, FLEX 8000, and FLEX 6000 devices.

CerDIP Ceramic dual in-line package. A device package offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* in this data book for more information.

Classic An Altera device family based on Altera's original EPROM-based EPLD architecture. The Classic™ device family includes the EP610, EP610I, EP910, EP910I, EP1800I, and EP1810 devices.

ClockBoost An Altera high-density programmable logic device feature available in selected FLEX 10K devices that uses a phase locked loop to increase clock frequencies by as much as four times the incoming clock rate, improving system performance. Combining the ClockBoost™ and ClockLock™ features provides significant advantages in system performance and bandwidth.

ClockLock An Altera high-density programmable logic device feature that uses a phase-locked loop (PLL) to minimize clock delay and skew within a device, significantly increasing performance. Combining the ClockLock and ClockBoost features provides significant advantages in system performance and bandwidth.

Compiler Netlist Extractor The MAX+PLUS II Compiler module that converts each design file in a project to a single database format. The Compiler Netlist Extractor also checks each design file in a project for problems such as duplicate node names, missing inputs and outputs, and outputs that are tied together.

Configuration EPROM Altera's family of serial EPROMs, which are designed to configure FLEX 10K, FLEX 8000, and FLEX 6000 devices. This device family includes the EPC1064, EPC1064V, EPC1213, EPC1441, and EPC1 devices.

configuration scheme The method used to load data into a FLEX devices.

Five configuration schemes are available for FLEX 10K devices: Configuration EPROM, passive serial (PS), passive parallel asynchronous (PPA), passive parallel synchronous (PPS), and JTAG. For complete information on FLEX 10K configuration schemes, see *Application Note 59 (Configuring FLEX 10K Devices)*.

Six configuration schemes are available for FLEX 8000 devices: active serial (AS), active parallel up (APU), active parallel down (APD), passive parallel asynchronous (PPA), passive parallel synchronous (PPS), and passive serial (PS). For complete information on FLEX 8000 configuration schemes, see *Application Note 33 (Configuring FLEX 8000 Devices)* and *Application*

Note 38 (Configuring Multiple FLEX 8000 Devices).

Three configuration schemes are available for FLEX 6000 devices: configuration EPROM, passive serial (PS), and passive serial asynchronous (PSA). For complete information on FLEX 6000 configuration schemes, see *Application Note 87 (Configuring FLEX 6000 Devices)*.

continuity checking A test for open circuits between device pins and programming adapter sockets. This test verifies that a device is properly seated in the socket of the adapter.

CQFP Ceramic quad flat pack. A device package offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* in this data book for more information.

D

Database Builder The MAX+PLUS II Compiler module that builds a single, fully flattened database that integrates all files in a project hierarchy. It also examines the logical completeness and consistency of the project and checks for boundary connectivity and syntactical errors.

dedicated input pin A pin that can only be used as an input to the device.

Design Doctor The Compiler utility that checks each design file in a project for logic that could cause reliability problems when the project is implemented in one or more devices. The Design Doctor runs in conjunction with the Logic Synthesizer module and analyzes the project with a predefined or customized set of design rules.

development socket A prototyping socket for high-pin-count QFP packages.

device Refers to an Altera programmable logic device, including FLEX 10K, FLEX 8000, FLEX 6000, MAX 9000, MAX 7000, MAX 5000, and Classic devices. Altera also offers Configuration EPROM devices that are used to configure FLEX 10K, FLEX 8000, and FLEX 6000 devices.

device family A group of Altera programmable logic devices with the same fundamental architecture. Altera device families include the FLEX 10K, FLEX 8000, FLEX 6000, MAX 9000, MAX 7000, MAX 5000, and Classic device families. Altera also offers a Configuration EPROM device family that includes devices used for configuring FLEX 10K, FLEX 8000, and FLEX 6000 devices.

DIP Dual in-line package. A device package offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* in this data book for more information. Ceramic (CerDIP) and plastic (PDIP) versions are available.

E

EDIF Electronic Design Interchange Format. An industry-standard format for the transmission of design data. You can generate an EDIF 2 0 0 or 3 0 0 netlist file from a schematic design or from a VHDL or Verilog HDL design that has been processed with an appropriate industry-standard synthesis tool. You can then import the file into the MAX+PLUS II software as an EDIF Input File (**.edf**). The MAX+PLUS II software supports EDIF Input Files that contain functions from the library of parameterized modules (LPM). The MAX+PLUS II Compiler can also generate one or more EDIF Output Files (**.edo**) in either EDIF 2 0 0 or 3 0 0 format that contain functional and timing information for simulation with a standard EDIF simulator.

EDIF Input File (.edf) An EDIF version 2 0 0 or 3 0 0 netlist file generated by any industry-

standard EDIF netlist writer. EDIF Input Files can be compiled by the MAX+PLUS II Compiler. The MAX+PLUS II software supports EDIF Input Files that contain functions from the library of parameterized modules (LPM).

EDIF Output File (.edo) An EDIF version 2 0 0 or 3 0 0 netlist file generated by the EDIF Netlist Writer module of the MAX+PLUS II Compiler. This file can be exported to an industry-standard UNIX workstation or PC environment for simulation.

EEPROM Electrically Erasable Programmable Read-Only Memory. A form of reprogrammable semiconductor memory in which the contents can be erased by subjecting the device to appropriate electrical signals. See *Operating Requirements for Altera Devices Data Sheet* and the *Configuration Elements & Reliability Data Sheet* in this data book for more information.

embedded array A series of embedded array blocks (EABs) that is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), microcontroller, wide data-path manipulation, and data transformation functions.

embedded array block (EAB) The building block of embedded arrays. Each EAB provides 2,048 bits of configurable RAM, ROM, FIFO, or dual-port RAM. When implementing logic, each EAB can contribute 100 to 300 gates towards complex logic functions.

EPLD Erasable programmable logic device. Altera EPLD device families include MAX 9000, MAX 7000, MAX 5000, and Classic.

EPROM Erasable Programmable Read-Only Memory. A form of reprogrammable semiconductor memory in which the contents can be erased by subjecting the device to the proper wavelength of ultraviolet light. See *Operating Requirements for Altera Devices Data Sheet* and the *Configuration Elements & Reliability Data Sheet* in this data book for more information.

expander product term A single product term with an inverted output that feeds back into the logic array block (LAB) of a MAX 9000, MAX 7000, or MAX 5000 device. An uncommitted expander product term that can be shared with other logic cells in the same LAB is called a shareable expander; a product term that has been shared in this manner is called a shared expander. In MAX 9000, and MAX 7000 devices only, an expander product term that is "borrowed" from an adjacent logic cell in the same LAB is called a parallel expander.

external timing parameters Factory-tested, worst-case values specified by Altera. In this data book, external timing parameters are shown in bold type. In the device family data sheets, external timing parameters are listed under "External Timing Characteristics."

extraction tool A tool to extract QFP devices from QFP carriers. Extraction tools are available from Altera for 100-, 160-, 208-, 240-, and 304-pin QFP packages. See the *QFP Carrier & Development Socket Data Sheet* in this data book for information.

F

FastFLEX I/O In the FLEX 6000 family, the FastFLEX™ I/O feature provides a direct path from LEs to an I/O pin for fast clock-to-output timing. See the *FLEX 6000 Programmable Logic Device Family Data Sheet* in this data book for more information.

Fast I/O A logic option you can use to specify that a register should be implemented in an I/O cell for FLEX 10K, FLEX 8000, MAX 9000, MAX 7000S, MAX 7000A, or MAX 7000E devices. This logic option can be applied to

individual logic functions. However, it cannot be incorporated into a logic synthesis style or applied to an entire project.

FastTrack Interconnect Dedicated connection paths that span the entire width and height of a FLEX 10K, FLEX 8000, FLEX 6000, or MAX 9000 device. The FastTrack™ Interconnect allows signals to travel between all logic array blocks (LABs) in a device.

Fit File (.fit) An ASCII text file generated by the Compiler that documents pin, logic cell, I/O cell, embedded cell, chip, and device assignments made during the last compilation.

Fitter The MAX+PLUS II Compiler module that fits a project into one or more devices. The Fitter selects appropriate interconnection paths as well as the pin and logic cell assignments. It also generates part of the Report File (**.rpt**) and Fit File (**.fit**) for the project.

FLASHlogic An Altera device family featuring SRAM-based devices with shadow EPROM or FLASH configuration elements. This family includes the EPX740, EPX780, EPX880, EPX8160 devices (devices in the FLASHlogic family are obsolete).

FLEX 6000 An Altera device family based on the OptiFLEX™ architecture. This SRAM-based family offers high-performance, register intensive, high-gate-count devices. The FLEX 6000 device family includes the EPF6016, EPF6016A, and EPF6024A devices.

FLEX 8000 An Altera device family based on the Flexible Logic Element MatriX (FLEX) architecture. This SRAM-based family offers high-performance, register-intensive, high-gate-count devices. The FLEX 8000 device family includes the EPF8282A, EPF8282AV, EPF8452A, EPF8636A, EPF8820A, EPF81188A, and EPF81500A devices.

FLEX 10K An Altera device family based on the Flexible Logic Element MatriX (FLEX) architecture. This SRAM-based family offers high-performance, register-intensive, high-gate-count devices with embedded arrays. The embedded arrays are used to efficiently implement memory or complex logic functions. The FLEX 10K device family includes the EPF10K10, EPF10K20, EPF10K30, EPF10K30A, EPF10K30B,EPF10K40, EPF10K50, EPF10K50B, EPF10K70, EPF10K100, EPF10K100A, EPF10K100B, EPF10K130B, EPF10K130V, EPF10K180B, EPF10K250A, EPF10K250B, and EPF10K50V devices.

flipflop An edge-triggered, clocked storage unit that stores a single bit of data. A low-to-high transition on the clock signal changes the output of the flipflop based on the value of the data input(s). This value is maintained until the next low-to-high transition of the clock, or until the flipflop is preset or cleared. Depending on the architecture of the device family, a register can be programmed as a level-sensitive flow-through latch or as an edge-triggered D, T, JK, or SR flipflop.

functional simulation A MAX+PLUS II Simulator mode that uses a functional Simulator Netlist File (**.snf**) to simulate the logical performance of a project without timing information.

Functional SNF Extractor The MAX+PLUS II Compiler module that creates the functional Simulator Netlist File (**.snf**) required for functional simulation.

G

Graphic Design File (.gdf) A schematic design file created with the MAX+PLUS II Graphic Editor.

global clear A signal from a dedicated input pin or logic element (LE) that does not pass through the logic array before arriving at the

clear input of a register. In FLEX 8000 devices, a global clear can come from any of the dedicated inputs. In FLEX 10K and FLEX 6000 devices, a global clear can come from any dedicated input or from a LE. MAX 9000 and MAX 7000 devices have input pins that can be used either as global clear sources or as dedicated inputs to the device.

global clock A signal from a dedicated input pin or logic element (LE) that does not pass through the logic array before arriving at the clock input of a register. In FLEX 8000 devices, a global clock can come from any of the four dedicated input pins. FLEX 10K, FLEX 8000, FLEX 6000, MAX 9000, MAX 7000, MAX 5000, and EP1810 devices have input pins that can be used as either global clock sources or dedicated inputs to the device. EP910 and EP610 devices have dedicated clock input pins. In FLEX 10K and FLEX 6000 devices, an LE can also generate a global clock signal.

H

Hexadecimal (Intel-Format) File (.hex) A hexadecimal file in the Intel Hex format. The MAX+PLUS II Compiler and Simulator can use Hex Files as inputs to specify the initial memory contents. After compilation, you can also create Hex Files that support configuration schemes for FLEX devices.

I

Include File (.inc) An ASCII text file that can be imported into a Text Design File (.**tdf**) with an AHDL Include Statement. The contents of the Include File replace the Include Statement that calls the file. Include Files can contain Function Prototype, Constant, Delete, and Parameters Statements.

internal timing parameters Worst-case delays based on external timing parameters. Internal timing parameters cannot be measured explicitly, and should only be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance. In this data book, internal timing parameters are shown in italics.

I/O cell Also known as an I/O element. A register that exists on the periphery of a FLEX 10K, FLEX 8000, or MAX 9000 device, or a fast input-type logic cell that is associated with an I/O pin in MAX 7000E, MAX 7000S, or MAX 7000A devices. I/O cells give short setup and clock-to-out times.

in-system programmability (ISP) The capability of EEPROM-based devices to be programmed after they have been mounted on a printed circuit board. Altera's MAX 9000, MAX 7000S, and MAX 7000A devices support ISP.

The MAX+PLUS II Programmer supports in-system programming via the BitBlaster serial download cable and the ByteBlaster parallel port download cable. The Programmer also provides the capability to program multiple devices in a JTAG chain.

J

Jam language An open-standard language for programming ISP-capable devices. The Jam™ language is supported by the MAX+PLUS II software version 8.0 and higher. Jam is an interpreted language that is optimized for programming devices via the Joint Test Action Group (JTAG) interface. The Jam language is platform independent, supports both new and existing ISP-capable devices, and has a small interpreter code and file size.

Jam File (.jam) An ASCII Jam device programming and test language file that stores programming data for programming, verifying, and blank-checking one or more ISP-capable devices in a JTAG chain. Jam Files are used in embedded processor or in-circuit test (ICT) equipment programming environments.

Altera's MAX 9000, MAX 7000S, and MAX 7000A devices can be programmed with Jam Files; FLEX 10K devices can be configured with Jam Files. In addition to the device(s) to be programmed or configured, the JTAG chain can contain any device that complies with the IEEE 1149.1 specification, including FLEX 10K, FLEX 6000, and some FLEX 8000 devices.

JEDEC File (.jed) An ASCII file that contains programming information. JEDEC Files provide an industry-standard format for transferring information between a data preparation system and a logic device programmer. The MAX+PLUS II Compiler automatically generates JEDEC Files for the following devices during compilation: EP610, EP610I, EP910, EP910I, and EP1810 devices (Classic family) as well as EPM5032 devices (MAX 5000 family). The MAX+PLUS II Programmer can use a JEDEC File created with the MAX+PLUS II software for DOS platforms, A+PLUS, or PLDshell Plus™ to program the Altera devices listed above, in addition to FLASHlogic devices (All FLASH devices are obsolete). The Programmer can also optionally save programming data plus functional test vectors in JEDEC File format.

JLCC Ceramic J-lead chip carrier. A device package offered by Altera. Both JLCC and plastic J-lead chip carrier (PLCC) packages are available. See the *Altera Device Package Information Data Sheet* and *Ordering Information* in this data book for more information.

JTAG Joint Test Action Group. A set of specifications that enables a designer to perform board- and device-level functional verification of a board during production.

JTAG boundary-scan testing Testing that isolates a device's internal circuitry from its I/O circuitry. This testing is made possible by the Joint Test Action Group (JTAG) boundary-scan test (BST) architecture that is available in all FLEX 10K devices, all FLEX 8000 devices except the EPF8452A and EPF81188A, and all FLEX 6000 devices, all MAX 9000, MAX 7000S, and MAX 7000A devices. Serial data is shifted into boundary-scan cells in the device; observed data is shifted out and externally compared to expected results. Boundary-scan testing offers efficient PC board testing, providing an electronic substitute for the traditional "bed of nails" test fixtures.

L

Library Mapping File (.lmf) An ASCII text file used to map cells in EDIF Input Files (.**edf**) or symbols in OrCAD Schematic Files (.**sch**) to corresponding MAX+PLUS II primitives, megafunctions, or macrofunctions.

library of parameterized modules (LPM) An architecture-independent library of logic functions that are parameterized to achieve scalability and adaptability. Altera has implemented parameterized modules from LPM version 2.0.1 to 2.1.0 that offer architecture-independent design entry for all MAX+PLUS II-supported devices. The MAX+PLUS II Compiler includes built-in compilation support for LPM functions used in schematics, AHDL TDFs, and EDIF Input Files.

linked simulation A MAX+PLUS II Simulator mode that uses a linked Simulator Netlist File (**.snf**) to simulate the logical performance of a super-project that consists of multiple, linked individual projects. A linked simulation uses the timing and/or functional netlist information from the combined SNFs of the individual linked sub-projects.

LPM *See* library of parameterized modules (LPM).

logic array A series of logic array blocks (LABs) that is used to implement general logic, such as counters, adders, state machines, and multiplexers. The logic array performs the same function as the sea-of-gates in gate arrays.

logic array block (LAB) A physically grouped set of logic resources in an Altera device. The LAB consists of a logic cell array and, in some device families, an expander product term array. Any signal that is available to any one logic cell in the LAB is available to the entire LAB. In FLEX 10K, FLEX 8000, FLEX 6000, and MAX 9000 devices, the LAB is fed by row interconnect paths and a dedicated input bus. In MAX 7000, MAX 7000A, and MAX 5000 devices, the LAB is fed by a programmable interconnect array (PIA) and a dedicated input bus. In Classic devices, the logic in the LAB shares a global clock signal. The LAB is fed by a global bus and a dedicated input bus. In the EP1810, LABs are called quadrants.

logic cell The generic term for the basic building block of an Altera device. In FLEX 10K, FLEX 8000, and FLEX 6000 devices, logic cells are called logic elements. In MAX 9000, MAX 7000, MAX 5000, and Classic devices, logic cells are called macrocells.

logic element (LE) A basic building block of FLEX 10K, FLEX 8000, and FLEX 6000 devices. A logic element consists of a look-up table (LUT)—i.e., a function generator that quickly computes any function of four variables—and a programmable register to support sequential functions. The register can be programmed as a flow-through latch, as a D, T, JK, or SR flipflop, or bypassed entirely for pure combinatorial logic. The register can feed other logic cells or feed back to the logic cell itself. Some logic elements feed output or bidirectional I/O pins on the device.

Logic Programmer card The expansion card required to run the MAX+PLUS II Programmer and program Altera devices. The MAX+PLUS II software currently supports the LP6 Programmer card for use with PCs.

Logic Synthesizer The Compiler module that uses several algorithms to minimize gate count, remove redundant logic, and utilize the device architecture as efficiently as possible. Processing can be customized with logic option and logic synthesis style assignments. This module also applies logic synthesis techniques to help implement timing requirements for a project.

look-up table (LUT) A function that generates outputs based on inputs and a set of stored data. The logic element of FLEX 10K, FLEX 8000, and FLEX 6000 devices includes a four-input LUT that can be configured to emulate any logical function of four inputs.

M

macrocell The basic building block in Altera MAX 9000, MAX 7000, MAX 5000, and Classic devices. A macrocell consists of two parts: combinatorial logic and a configurable register. The combinatorial logic can implement a wide variety of logic functions. Depending on the architecture of the device family, the register can be programmed as a flow-through latch, as a D, T, JK, or SR flipflop, or bypassed entirely for pure combinatorial logic. The register can feed other macrocells or feed back to the macrocell itself. Some macrocells feed output or bidirectional I/O pins on the device. Macrocells in FLEX 10K, FLEX 8000, and FLEX 6000 devices are called logic elements.

macrofunction A high-level building block that can be used together with gate and flipflop primitives in MAX+PLUS II design files. In general, a macrofunction is a lower-level design file in a MAX+PLUS II hierarchical project.

Master Programming Unit (MPU) A hardware module that works with zero-insertion-force sockets and individual adapters to program and test Altera devices. The PL-MPU base unit and PLM-prefix adapters support both device programming and device testing. The PLE3-12 base unit, as well as adapters with other prefixes, support device programming only.

MAX 5000 An Altera device family based on the first generation of Multiple Array MatriX (MAX) architecture. This EPROM-based device family includes EPM5032, EPM5064, EPM5128, EPM5130, and EPM5192 devices.

MAX 7000 An Altera device family based on the second generation of Multiple Array MatriX (MAX) architecture. MAX 7000A, MAX 7000S, and MAX 7000E devices are enhanced versions of MAX 7000 devices and are function-, pin-, and programming file-compatible with MAX 7000 devices. MAX 7000A, MAX 7000E, and MAX 7000S devices offer up to six pin- or logic-driven output enable signals, fast input setup times to logic cells, and multiple global clocks with optional inversion. In addition, MAX 7000S and MAX 7000A devices feature ISP and JTAG boundary-scan test circuitry. The MAX 7000A devices are also optimized for 3.3-V operation. These EEPROM-based devices include EPM7032, EPM7032S, EPM7032V, EPM7032A, EPM7064, EPM7064S, EPM7064A, EPM7096, EPM7128E, EPM7128S, EPM7128A, EPM7160E, EPM7160S, EPM7192E, EPM7192S, EPM7256E, EPM7256S, EPM7256A, EPM7384A, EPM7512A, and EPM71024A devices.

MAX 9000 An Altera device family based on the third generation of Multiple Array MatriX (MAX) architecture, with a higher density than the MAX 7000 device family. These EEPROM-based devices include EPM9320, EPM9320A, EPM9400, EPM9480, EPM9480A, EPM9560, and EPM9560A devices.

MAX+PLUS II Altera's Multiple Array MatriX Programmable Logic User System. The MAX+PLUS II software is a set of computer programs and hardware support products that allow design and implementation of custom logic with FLEX 10K, FLEX 8000, FLEX 6000, MAX 9000, MAX 7000, MAX 5000, and Classic devices.

MegaCore function Altera-created megafunctions that are optimized for use with Altera devices. MegaCore™ functions are add-on products to the MAX+PLUS II software.

megafunction An off-the-shelf building block that implements useful functions such as processors, digital signal processing (DSP) functions, bus controllers, and interfaces. Both MegaCore and AMPP megafunctions are available.

MultiVolt feature An interface that separates the power supply from the output voltage, enabling Altera devices powered at a specific core voltage level to interface with devices using different voltage levels. For example, Altera's FLEX 10KA family, which has the MultiVolt™ feature, supports 5.0-V, 3.3-V, and 2.5-V levels.

O

OptiFLEX architecture The FLEX 6000 family features this highly efficient programmable logic architecture, which is targeted at producing maximum performance and utilization in the smallest possible die area. See the *FLEX 6000 Programmable Logic Device Family Data Sheet* in this data book for more information.

OrCAD Library File (.lib) A binary file containing information that describes how symbols are displayed in OrCAD Schematic Files (.**sch**).

OrCAD Schematic File (.sch) A schematic design file created with the OrCAD Draft schematic editor. You can open and edit an OrCAD Schematic File in MAX+PLUS II and save it as both a Graphic Design File (.**gdf**) and an OrCAD Schematic File (.**sch**). An OrCAD Schematic File can also be compiled directly by the MAX+PLUS II Compiler.

P

parallel expander An expander product term that is "borrowed" from an adjacent logic cell in the same MAX 9000 or MAX 7000 logic array block (LAB). A parallel expander is also a logic option that you can apply to a logic function to allow it to borrow such parallel expanders. This option can reduce the number of shared expander product terms required in your project and increase the speed of your project. However, the project may use additional logic cells, and may be more difficult to fit.

Partitioner The MAX+PLUS II Compiler module that divides a project into multiple devices, minimizing the number of connections between devices.

passive parallel asynchronous (PPA) A configuration scheme in which an external controller (e.g., a CPU) loads the design data into a FLEX 10K or FLEX 8000 device via a common data bus.

PCI *See* peripheral component interconnect (PCI).

PDIP Plastic dual in-line package. A device package offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* in this data book for more information.

peripheral component interconnect (PCI) An industry-established, high-speed bus standard for 32- and 64-bit applications.

PGA Pin-grid array. A ceramic device package offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* in this data book for more information.

PIA *See* programmable interconnect array.

PQFP Plastic quad flat pack. A device package offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* in this data book for more information.

PLAD3-12 An adapter that plugs into the Master Programming Unit (MPU). This adapter allows you to use PLE-prefix adapters originally designed for use with the PLE3-12A programming unit.

PLCC Plastic J-lead chip carriers. A device package option offered by Altera. Both ceramic J-lead chip carrier (JLCC) and PLCC packages are available.

PLDshell Plus Altera's Programmable Logic Shell. The PLDshell Plus software is a set of computer programs for designing and implementing custom logic circuits for Altera FLASHlogic and Classic devices. The MAX+PLUS II Programmer can program FLASHlogic and Classic devices with JEDEC Files (**.jed**) created by PLDshell Plus. All FLASHlogic devices are obsolete.

programmable interconnect array (PIA) The portion of a MAX 7000 or MAX 5000 device that routes signals between different logic array blocks (LABs).

product term Two or more factors in a Boolean expression combined with an AND operator constitute a product term, where "product" means "logic product."

Programmer Object File (.pof) A binary file generated by the MAX+PLUS II Compiler's Assembler module. This file contains the data used by the MAX+PLUS II Programmer to program an Altera device. The MAX+PLUS II Programmer can optionally save functional test vectors in a POF.

programmable logic devices (PLDs) Digital, user-configurable integrated circuits used to implement custom logic functions. PLDs can implement any Boolean expression or

registered function with built-in logic structures.

programming file A file containing data for programming Altera devices. Both the MAX+PLUS II Compiler and Programmer can generate programming files. The following programming file formats are available in MAX+PLUS II: FLEX Chain File (**.fcf**), Hexadecimal (Intel-Format) File (**.hex**), Jam File (**.jam**), JEDEC File (**.jed**), JTAG Chain File (**.jcf**), Programmer Object File (**.pof**), Raw Binary File (**.rbf**), Serial Bitstream File (**.sbf**), Serial Vector Format File (**.svf**), SRAM Object File (**.sof**), and Tabular Text File (**.ttf**).

FLEX Chain Files, JTAG Chain Files, Programmer Object Files, SRAM Object Files, and JEDEC Files are used to program or configure devices with the MAX+PLUS II Programmer. Test vectors for functional testing can be saved in POFs and JEDEC Files. All other file formats are used to configure FLEX 10K, FLEX 8000, and FLEX 6000 devices by other means. JTAG Chain Files are used to program or configure one or more FLEX 10K, MAX 9000, MAX 7000S, or MAX 7000A devices in a multi-device JTAG chain. The Programmer can save data read from an examined device in POF or JEDEC File format.

project A project consists of all files associated with a particular design, including all subdesign files and related ancillary files created by the user or by the MAX+PLUS II software. The project name is the same as the name of the top-level design file in the project, without the filename extension. The MAX+PLUS II software performs compilation, simulation, timing analysis, and programming on only one project at a time.

Q

QFP Quad flat pack. A device package offered by Altera. Windowed ceramic QFP (CQFP), plastic QFP (PQFP), power QFP (RQFP), and plastic thin QFP (TQFP) packages are available. See the *Altera Device Package Information Data Sheet* and *Ordering Information* in this data book for more information.

R

register *See* flipflop.

removal tool *See* extraction tool.

Report File (.rpt) An ASCII text file, generated by the MAX+PLUS II Compiler's Fitter module, that shows how device resources are used by the project. If a module preceding the Partitioner generates an error, this file is not generated. If the Partitioner generates an error, the Report File is generated in most cases.

RQFP Power quad flat pack. A device package offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* in this data book for more information.

S

security bit A bit that prevents an EPROM- or EEPROM-based Altera device from being interrogated. This bit also prevents EPROM-based Altera devices from being inadvertently reprogrammed. The security bit can be turned on or off for each device in a project, or for the entire project.

shared expanders and **shareable expanders** A feature of the MAX 9000, MAX 7000, MAX 7000A, and MAX 5000 device architecture that allows logic cells to use uncommitted product terms within the same logic array block (LAB). A product term that is eligible to be shared in this manner is called a sharable expander; a product term that has been shared in this manner is called a shared expander. The MAX+PLUS II Compiler automatically allocates shareable expanders when a project is compiled. A shared expander also can be allocated with an EXP primitive.

Simulator Netlist File (.snf) A binary file containing the data for functional simulation, timing simulation or timing analysis, or linked multi-device simulation. Three optional Compiler modules create the different types of SNFs that contain the information required for different simulation modes and/or timing analysis.

SOIC Small-outline integrated circuit. A plastic device package option. See the *Altera Device Package Information Data Sheet* and *Ordering Information* in this data book for more information.

SRAM Static random access memory. A read-write memory that stores data in integrated flipflops. See the *Configuration Elements & Reliability Data Sheet* in this data book for more information.

SRAM Object File (.sof) A binary file generated by the MAX+PLUS II Compiler's Assembler module that contains the data for configuring Altera FLEX 10K, FLEX 8000, or FLEX 6000 devices.

Symbol File (.sym) A graphic file created by the Symbol Editor or the Compiler Netlist Extractor module of the Compiler. This file represents a design file (a megafunction or macrofunction) or MAX+PLUS II primitive with the same name and can be used in Graphic Design Files (.**gdf**).

T

TabulPar Text File (.ttf) An ASCII text file in tabular format containing configuration data for the sequential passive parallel synchronous (PPS), passive parallel asynchronous (PPA), and passive serial (PS) configuration schemes for FLEX 8000 devices, and the PS configuration scheme for FLEX 10K devices.

Text Design Export File (.tdx) An ASCII text file in the Altera Hardware Description Language (AHDL) format that is optionally generated when you compile a Xilinx Netlist Format File (.**xnf**). It contains the same logic as the XNF File. A Text Design Export File can be saved as a Text Design File (.**tdf**) and used to replace the corresponding XNF File in the hierarchy of a project.

Text Design File (.tdf) An ASCII text file written in AHDL format. Text Design Export Files (.**tdx**) and Text Design Output Files (.**tdo**) can be saved as TDFs and compiled with the MAX+PLUS II software.

Text Design Output File (.tdo) An ASCII text file in AHDL format that is optionally generated when you compile any design. It contains a cell-by-cell description of the design as by the MAX+PLUS II software.

timing simulation A MAX+PLUS II Simulator mode that uses a timing Simulator Netlist File (**.snf**) to simulate the logical and timing performance of a project. Because the timing SNF is generated after logic synthesis, partitioning and fitting are performed, timing simulation allows you to simulate only the nodes in a project that have not been removed by logic optimization.

TQFP Plastic quad flat pack. A device package offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* in this data book for more information.

Turbo Bit A control bit for choosing the speed and power characteristics of an Altera device. If the Turbo Bit™ feature is on, the speed increases; if it is off, the power consumption decreases. The Turbo Bit feature can be turned on or off in a design file or in the Compiler.

U

user I/O The total number of I/O pins and dedicated inputs on a device.

V

Verilog HDL A hardware description language (HDL) from Cadence. You can create a Verilog HDL description with the MAX+PLUS II Text Editor or any standard text editor and compile it directly with the MAX+PLUS II software. You can also generate an EDIF 2 0 0 or 3 0 0 netlist file from a Verilog HDL design that has been processed with a Verilog HDL synthesis tool. The netlist file can then be imported into the MAX+PLUS II software as an EDIF Input File (**.edf**). The MAX+PLUS II Compiler can also generate a Verilog Output File (**.vo**).

Verilog Output File (.vo) A Verilog HDL standard netlist file generated by the Verilog Netlist Writer module of the Compiler. A Verilog Output File contains functional and timing information for simulation with a standard Verilog HDL simulator.

VHDL Very High Speed Integrated Circuit (VHSIC) Hardware Description Language. You can create a VHDL Design File (**.vhd**) with the MAX+PLUS II Text Editor or any standard text editor and compile it directly with the MAX+PLUS II software. You can also generate an EDIF 2 0 0 or 3 0 0 netlist file from a VHDL design that has been processed with a VHDL synthesis tool. The netlist file can then be imported into the MAX+PLUS II software as an EDIF Input File (**.edf**). The MAX+PLUS II Compiler can also generate a VHDL Output File (**.vho**).

VHDL Design File (.vhd) An ASCII text file created with the MAX+PLUS II Text Editor or another standard text editor. The VHDL Design File contains design logic that is defined with VHDL.

VHDL Output File (.vho) A VHDL standard netlist file that is generated by the VHDL Netlist Writer module of the Compiler. A VHDL Output File contains functional and timing information for simulation with a standard VHDL simulator.

W

Waveform Design File (.wdf) A binary file created with the MAX+PLUS II Waveform Editor, which contains design logic that is defined by a combination of waveforms.

X

Xilinx Netlist Format (.xnf) A netlist format generated by Xilinx software. XNF Files generated by running the Xilinx LCA2XNF utility can be compiled directly by the MAX+PLUS II Compiler. An XNF File can define all logic in a project, or be incorporated at the bottom level in a hierarchical project.